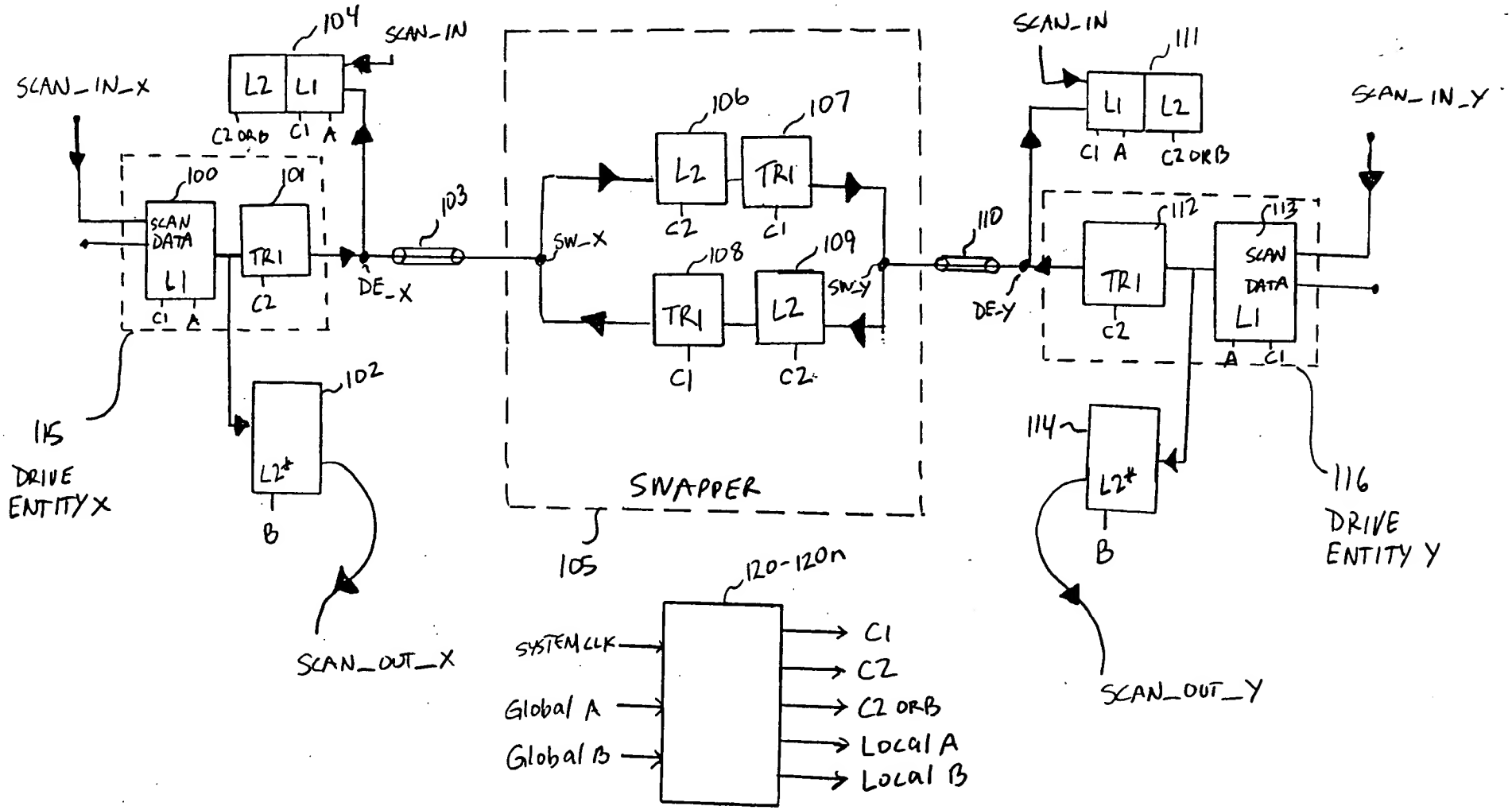


FIG. 1A

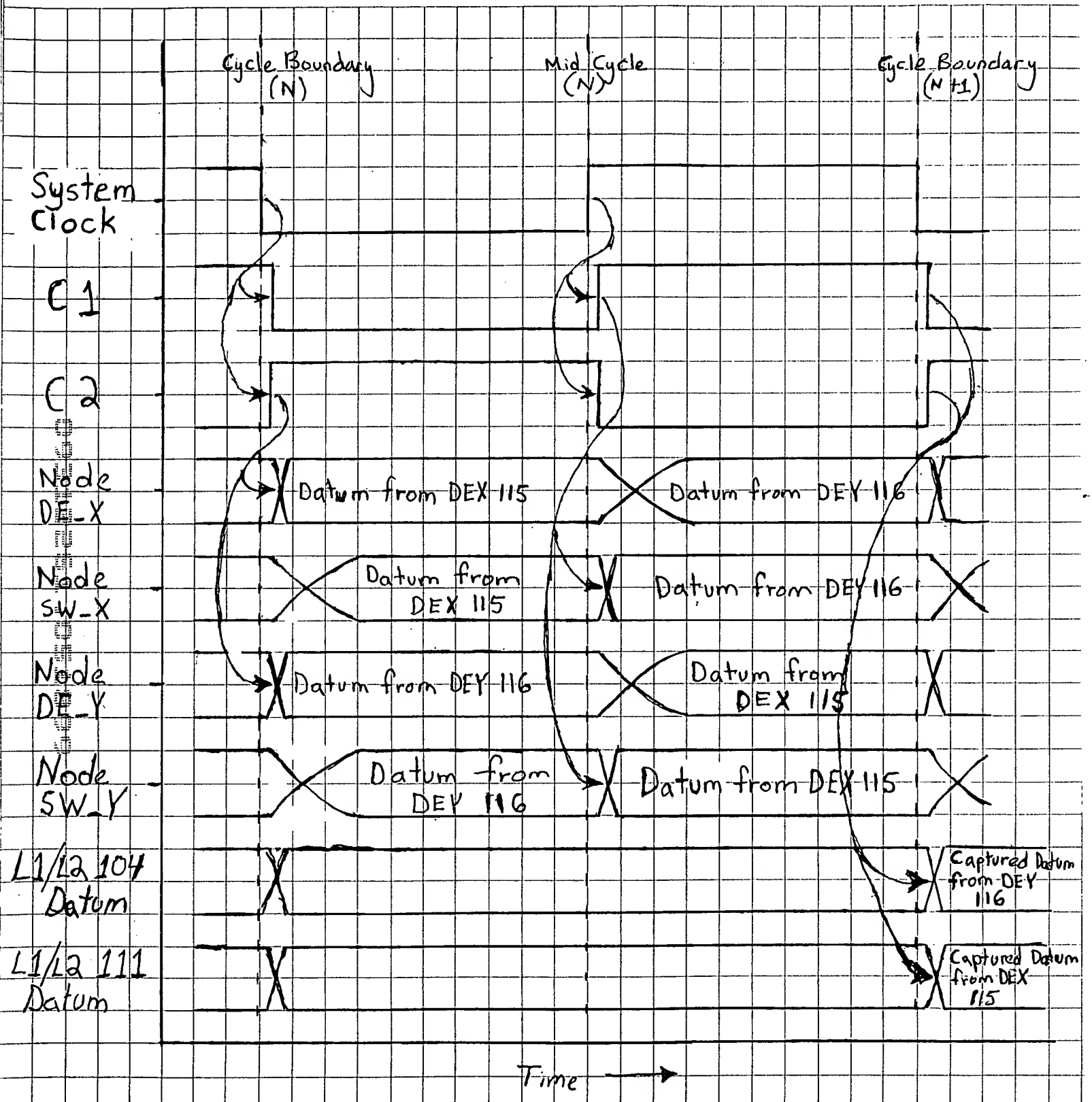


Figure 1B

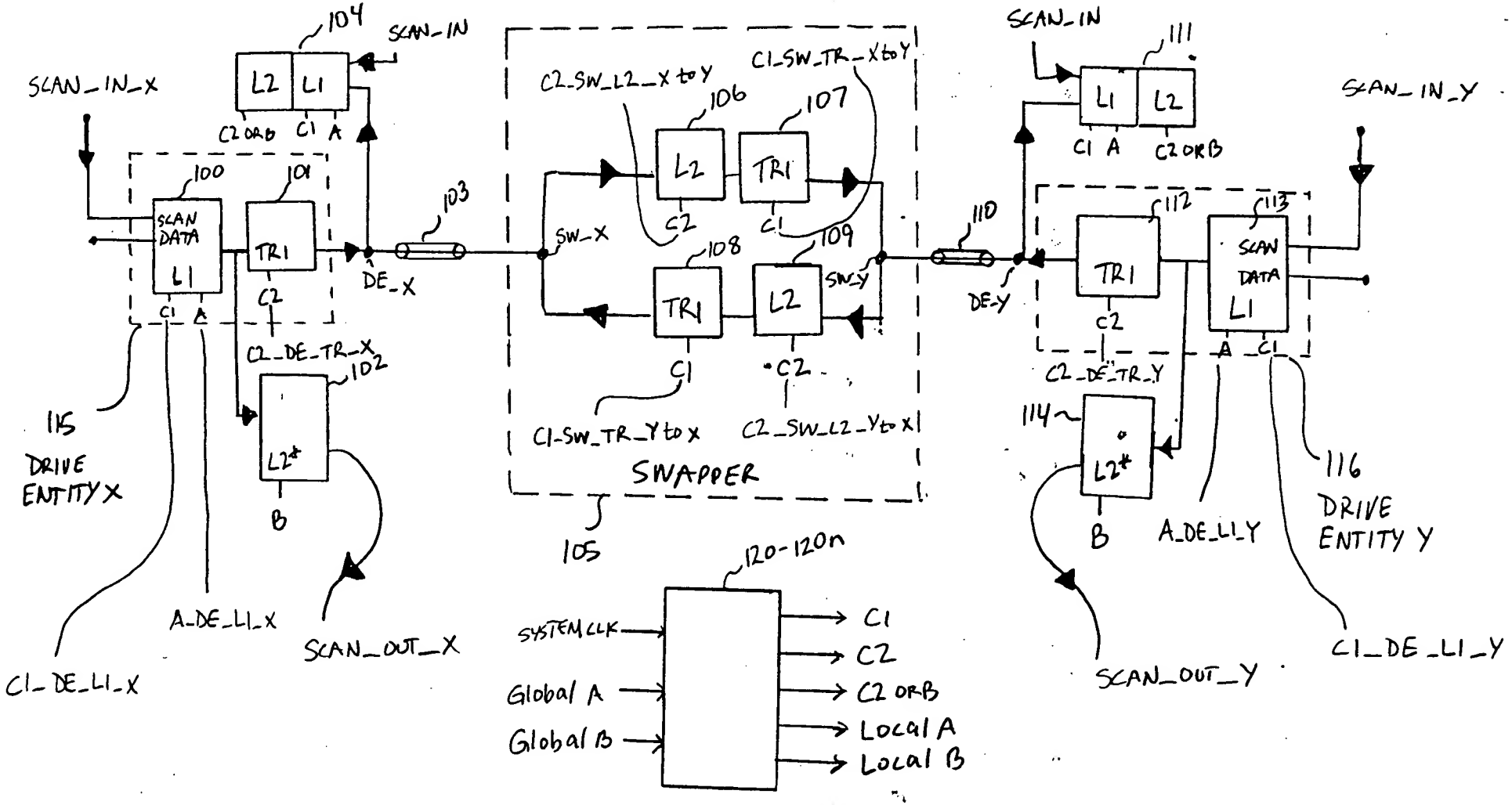

SCAN_IN_X
104
SCAN_IN
L2
L1
C2 OR B
C1
A
100
101
SCAN DATA
L1
TRI
C2
C1
A
103
DE_X
C2_DE_TR_X
102
L2*
B
115
DRIVE ENTITY X
A_DE_L1_X
C1_DE_L1_X
SCAN_OUT_X
SW_X
C2_SW_L2_X to Y
C1_SW_TR_X to Y
106
107
L2
TRI
C2
C1
108
109
TRI
L2
SW_Y
C1
C2
C1_SW_TR_Y to X
C2_SW_L2_Y to X
SWAPPER
105
110
DE_Y
SCAN_IN
111
L1
L2
C1
A
C2 OR B
SCAN_IN_Y
112
113
TRI
SCAN DATA
L1
C2
A
C1
C2_DE_TR_Y
114
L2*
B
A_DE_L1_Y
116
DRIVE ENTITY Y
C1_DE_L1_Y
SCAN_OUT_Y
120-120n
SYSTEM CLK
Global A
Global B
C1
C2
C2 OR B
Local A
Local B

FIG. 1C

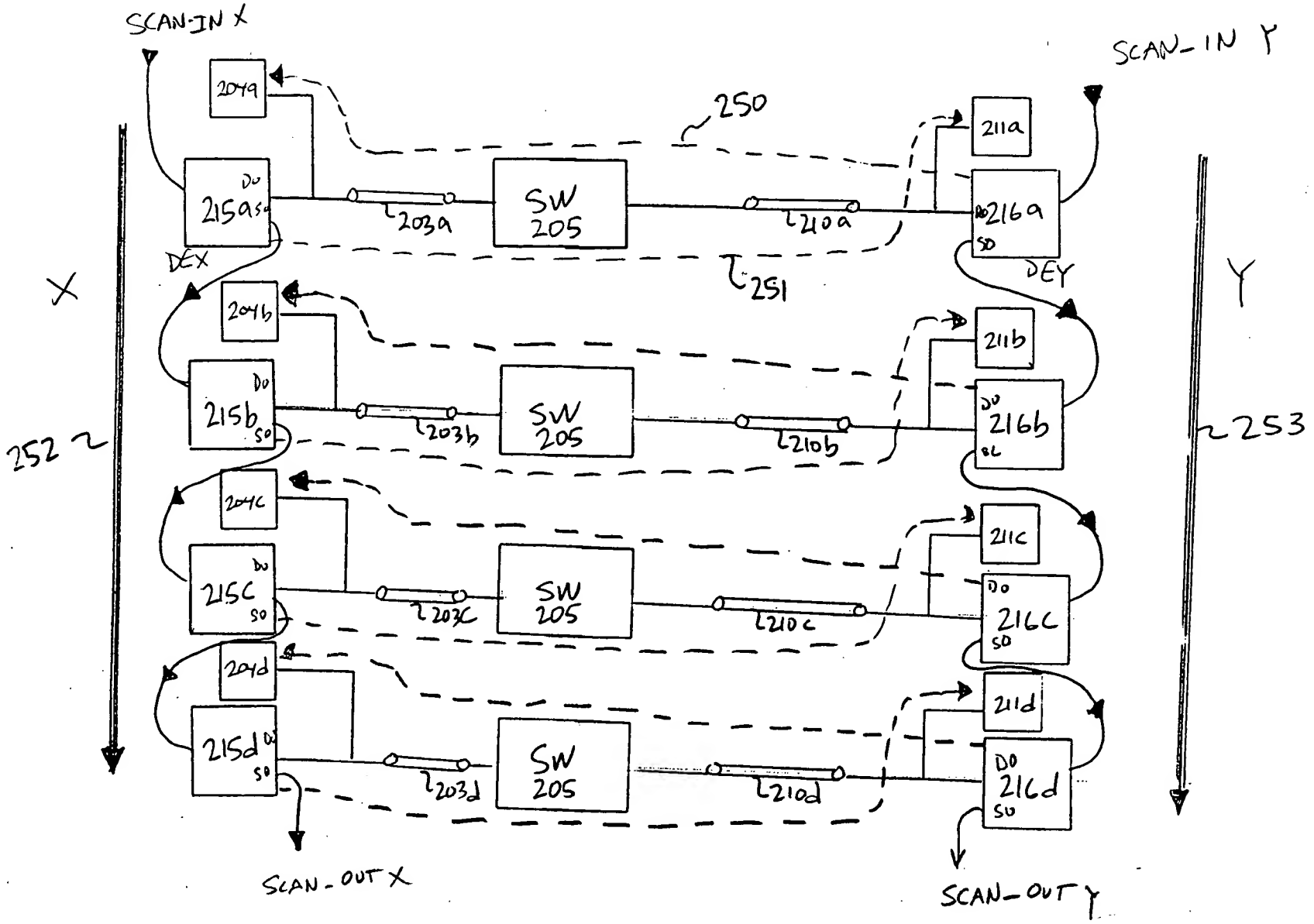

SCAN-IN X
SCAN-IN Y
250
204a
211a
215a
DO
SO
203a
SW
205
210a
216a
DEX
251
DEY
204b
211b
215b
203b
210b
216b
204c
211c
215c
203c
210c
216c
204d
211d
215d
203d
210d
216d
X
252
Y
253
SCAN-OUT X
SCAN-OUT Y

FIG 2A

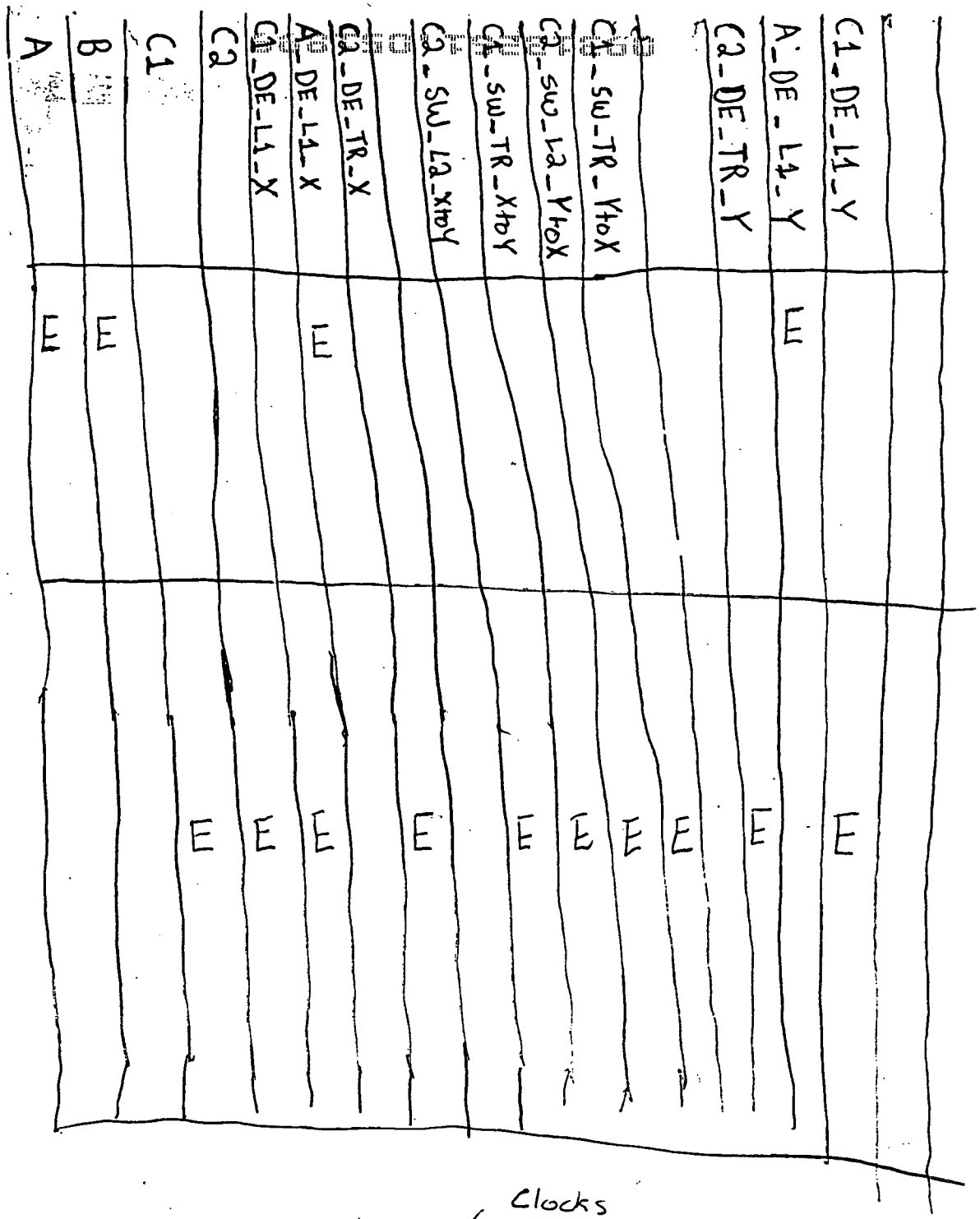


Figure 2B

E = Enabled

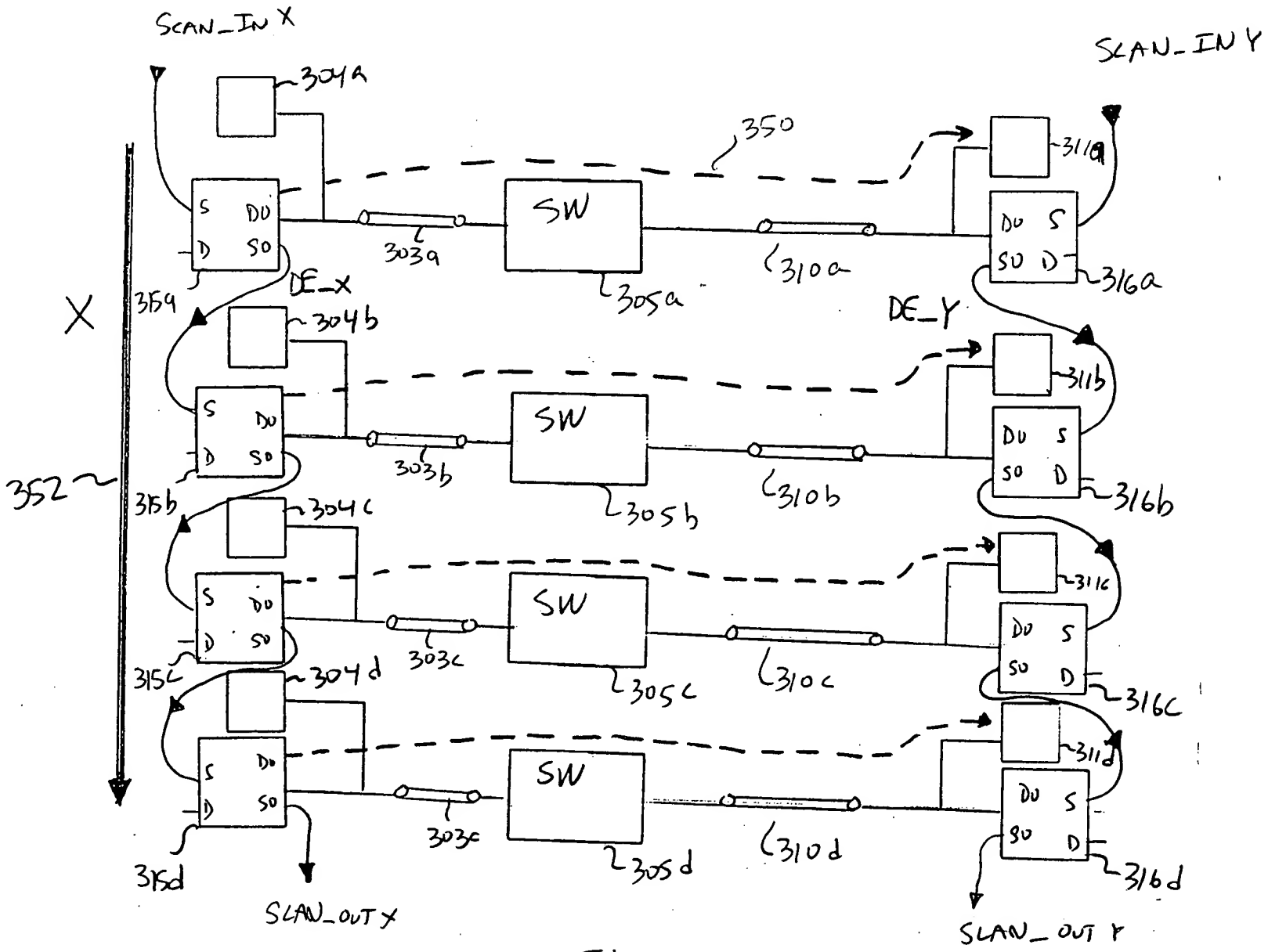


FIG 3A

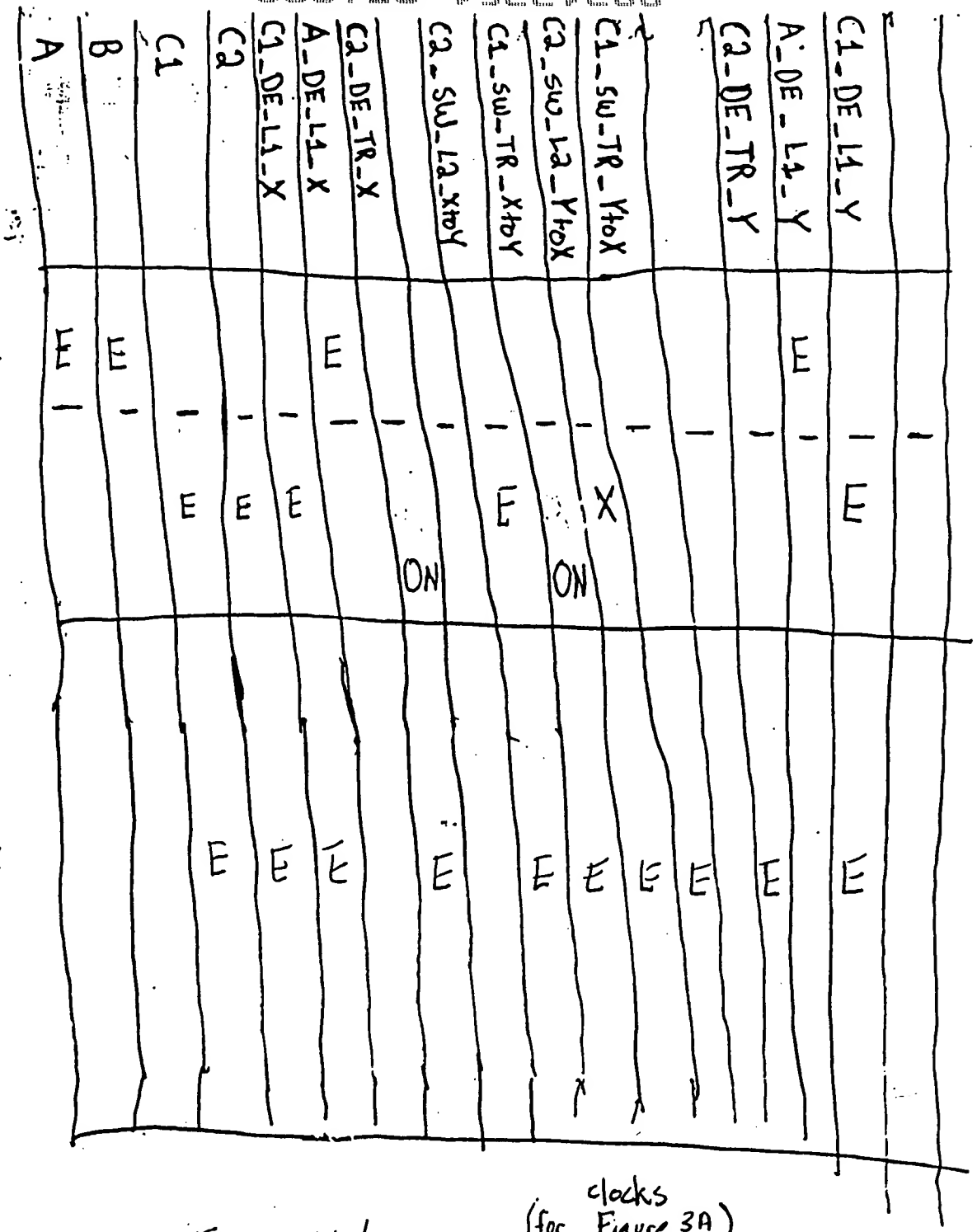


Figure 3B

E = Enabled

clocks (for Figure 3A)

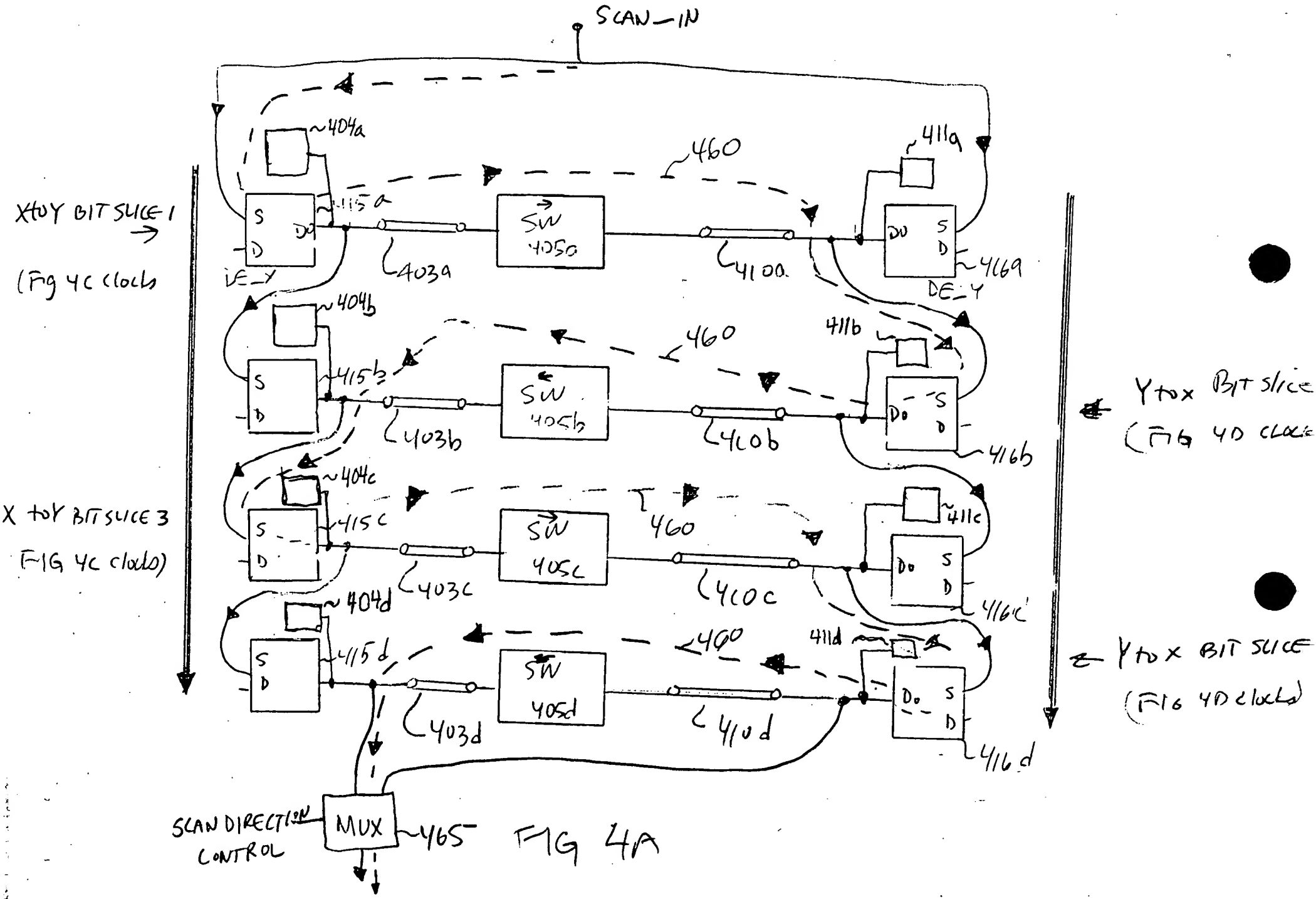

SCAN_IN
404a
460
411a
X to Y BIT SLICE 1
(Fig 4C clock)
S
D
Do
415a
SW
405a
403a
410a
411a
DE_Y
404b
460
411b
415b
SW
405b
403b
410b
411b
Y to X BIT SLICE
(Fig 4D clock
404c
415c
SW
405c
460
411c
X to Y BIT SLICE 3
FIG 4C clock)
403c
410c
411c
404d
415d
460
411d
SW
405d
403d
410d
411d
Y to X BIT SLICE
(FIG 4D clock)
SCAN DIRECTION CONTROL
MUX
465

FIG 4A

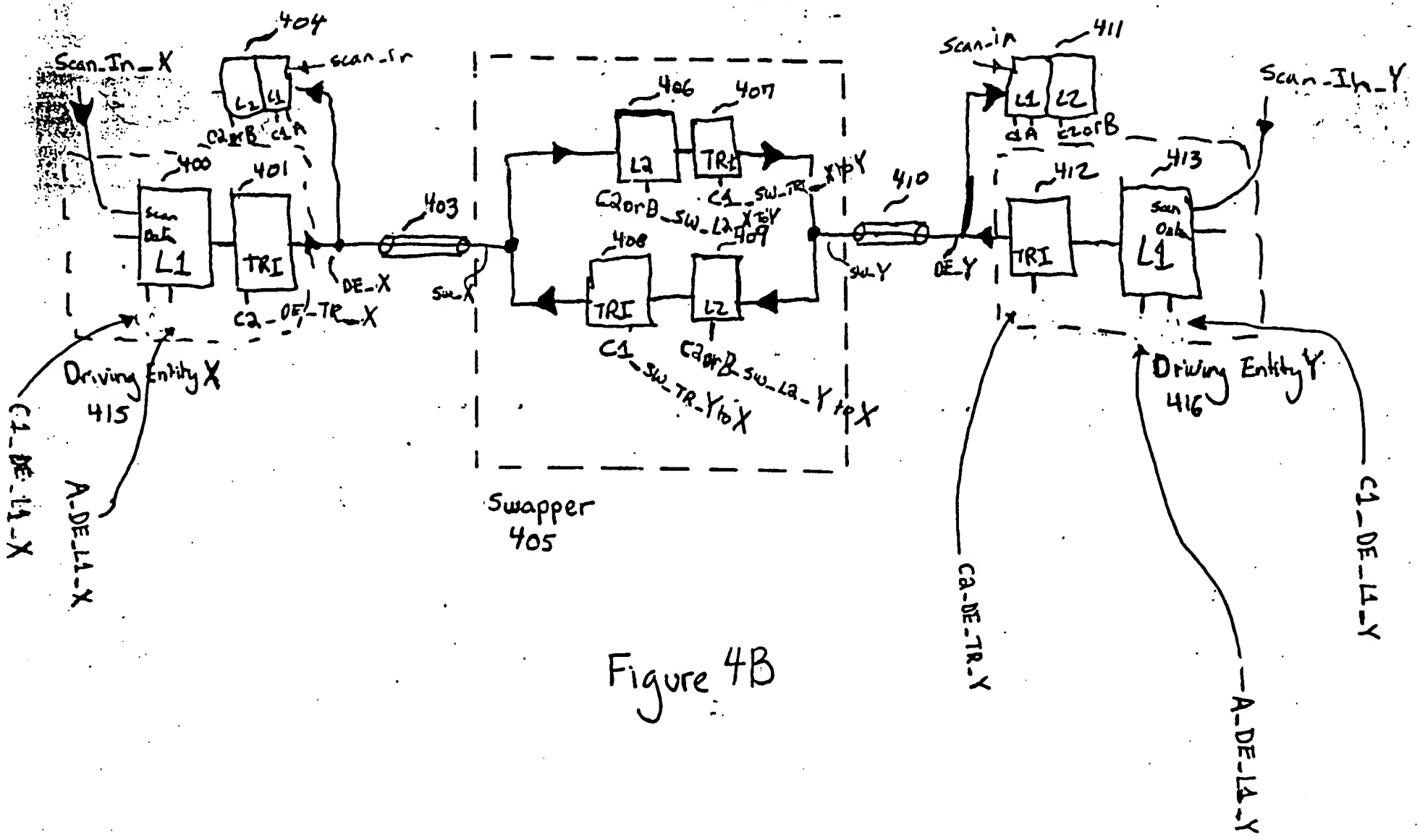
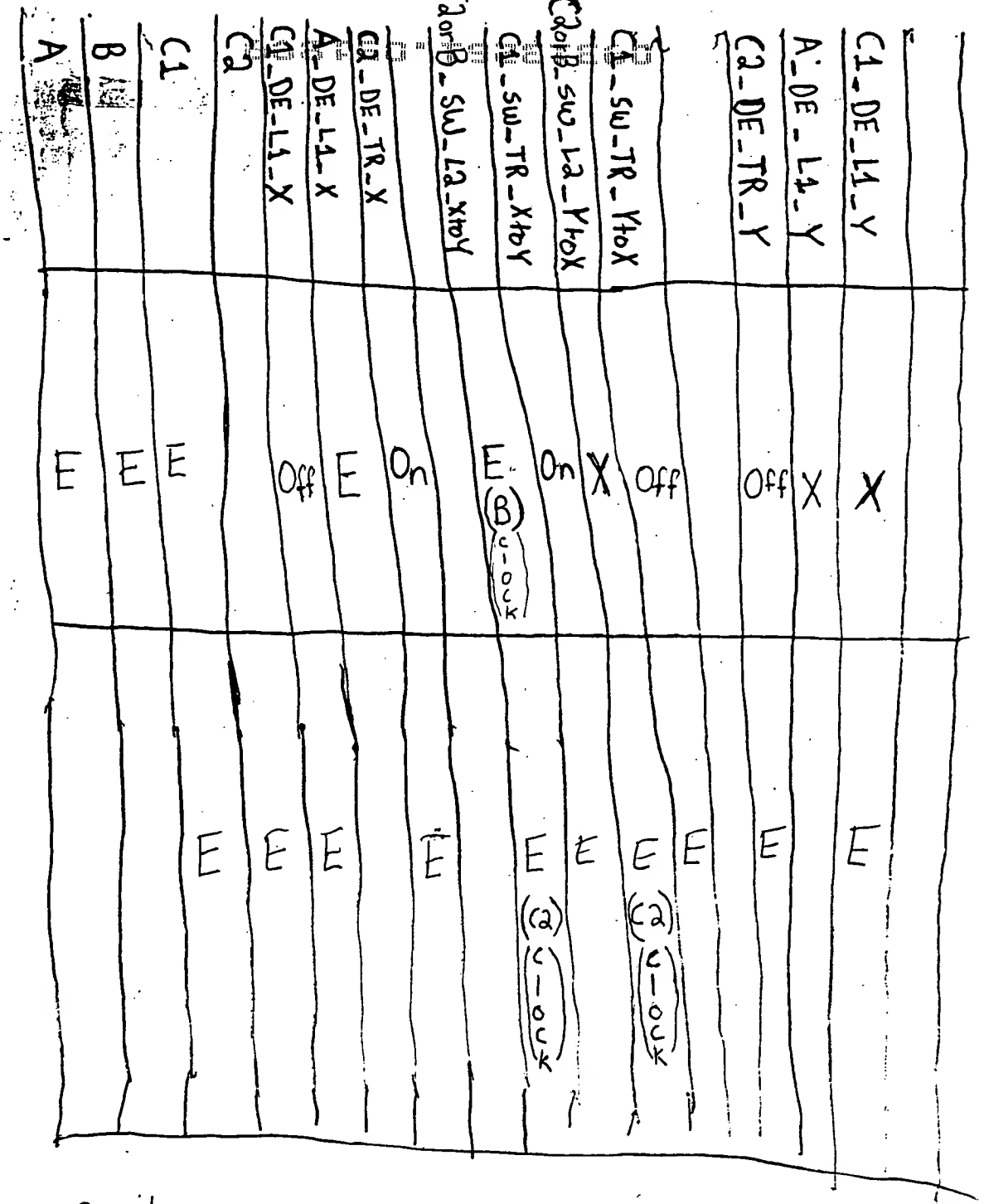

Scan_In_X
404
L2
L1
C2orB
C1A
scan_in
400
401
L1
TRI
403
DE_X
C2_DE_TR_X
SW_X
406
407
L2
TRI
C2orB_SW_L2_X to Y
C1_SW_TR_X to Y
408
409
TRI
L2
C1_SW_TR_Y to X
C2orB_SW_L2_Y to X
410
SW_Y
DE_Y
411
scan_in
L1
L2
C1A
C2orB
412
TRI
413
scan Out
L1
Scan_In_Y
Driving Entity X
415
A_DE_L1_X
C1_DE_L1_X
Swapper
405
C2_DE_TR_Y
A_DE_L1_Y
C1_DE_L1_Y
Driving Entity Y
416

Figure 4B



Clocks for XtoY ~~Byte~~ transfer

Figure 4C

	Combined Scan and Test Modes	System Mode
C1_DE_L1_Y	Off	E
A_DE_L1_Y	E	E
C2_DE_TR_Y	On	
		E
C1_SW_TR_YtoX	On	E (C2 clock)
C2orB_SW_L2_YtoX	E (B clock)	E
C1_SW_TR_XtoY	Off	E (C2 clock)
C2orB_SW_L2_XtoY	X	
C2_DE_TR_X	Off	E
A_DE_L1_X	X	E
C1_DE_L1_X	X	E
C2		E
C1	E	
B	E	
A	E	

Clocks for XtoY ~~Bypass~~ transfer

Figure 4D

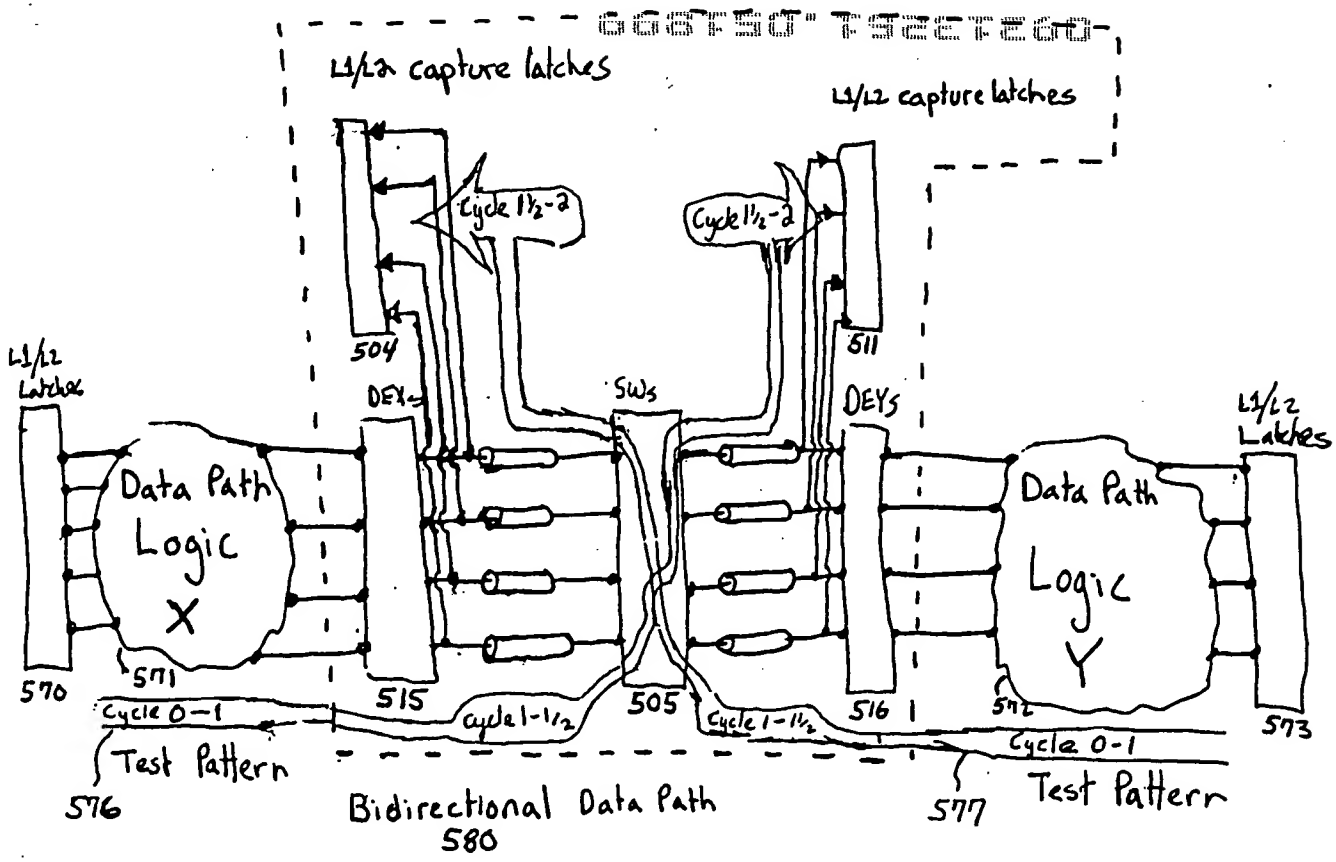
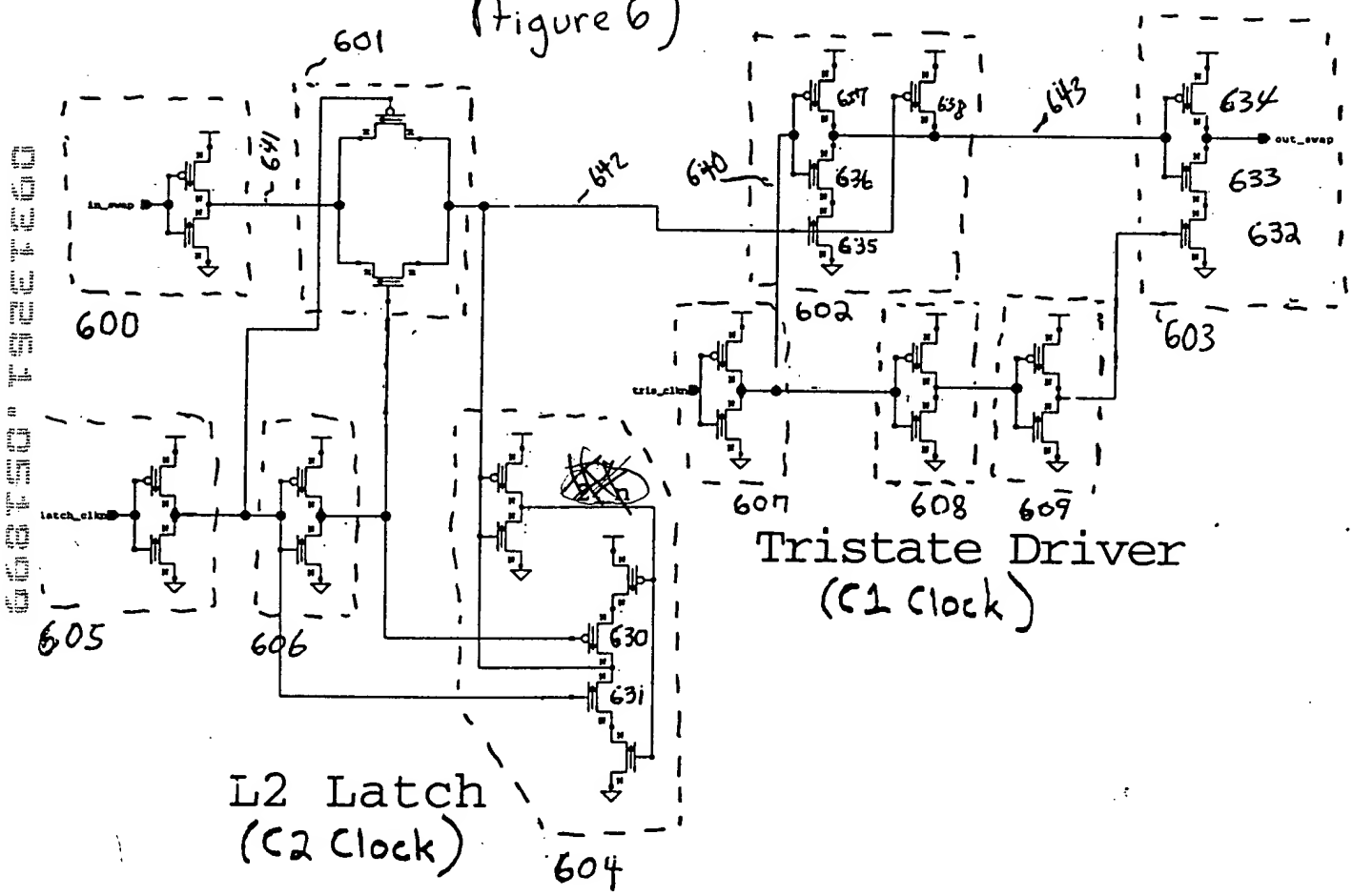

L1/L2 capture latches
L1/L2 capture latches
Cycle 1½-2
Cycle 1½-2
504
511
L1/L2 Latches
DEX
SWS
DEY
L1/L2 Latches
Data Path Logic X
Data Path Logic Y
570
571
515
505
516
572
573
Cycle 0-1
Cycle 1-1½
Cycle 1-1½
Cycle 0-1
Test Pattern
Test Pattern
576
Bidirectional Data Path
580
577

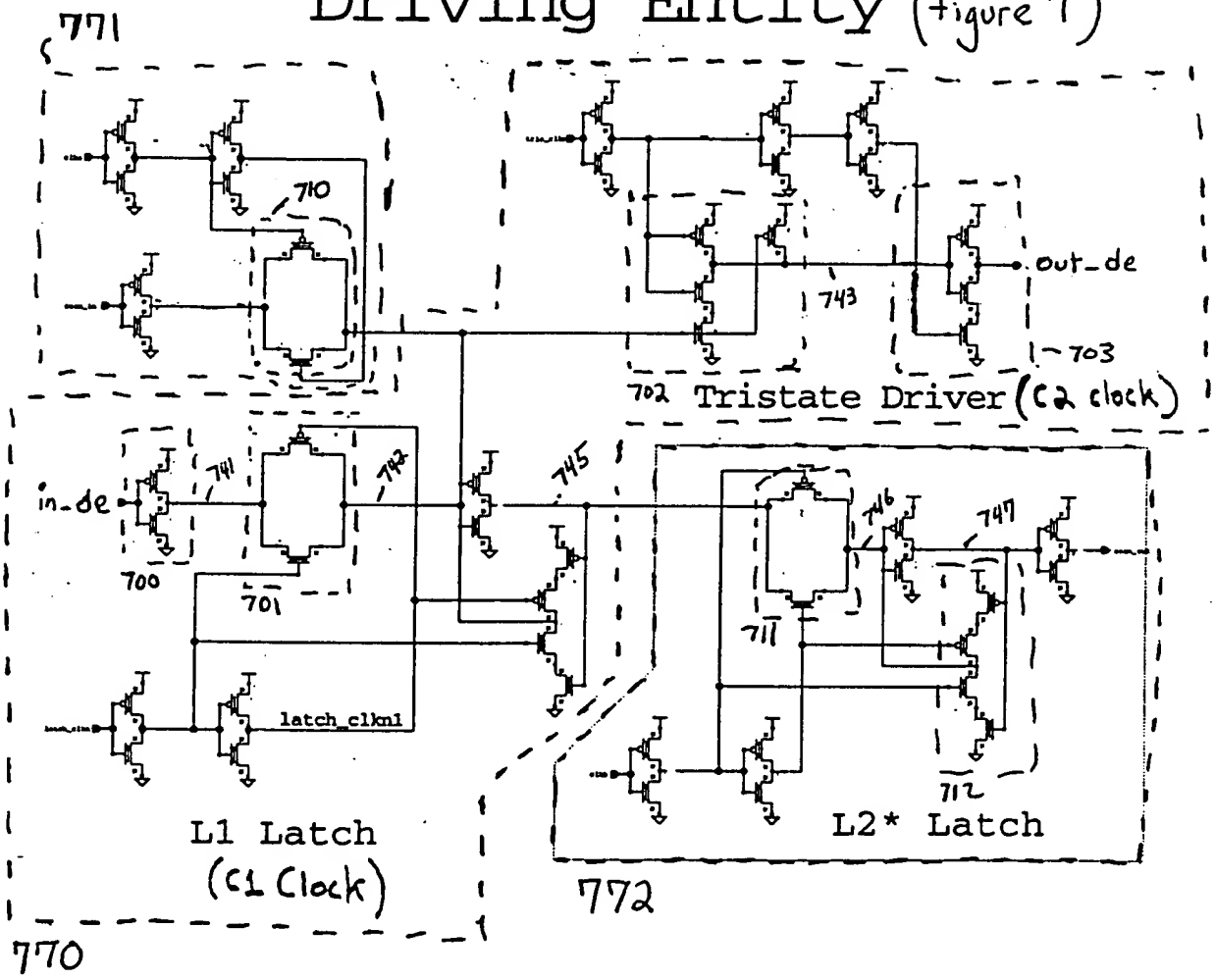
Figure 5

Half Swapper

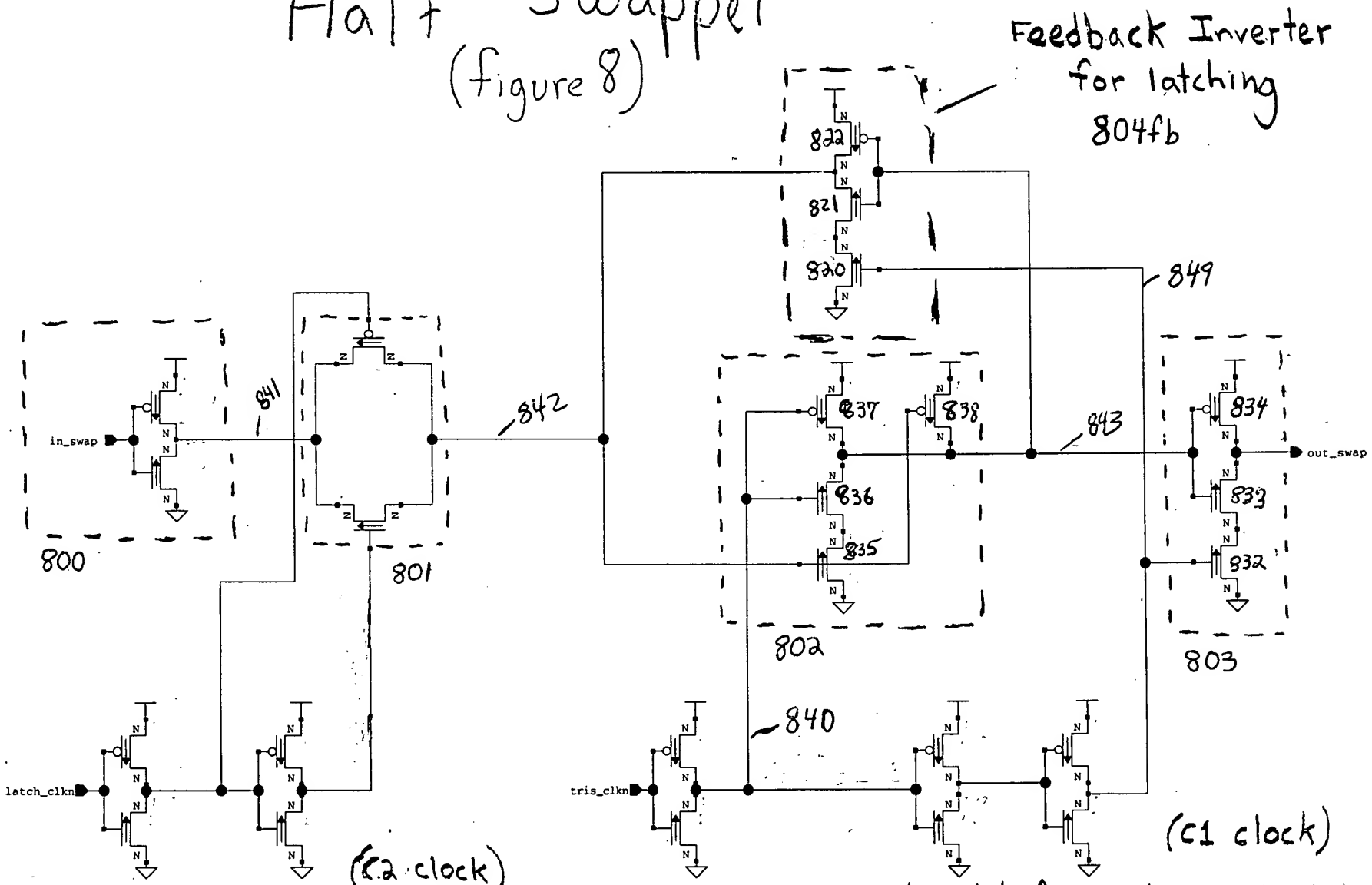
(figure 6)



Driving Entity (figure 7)

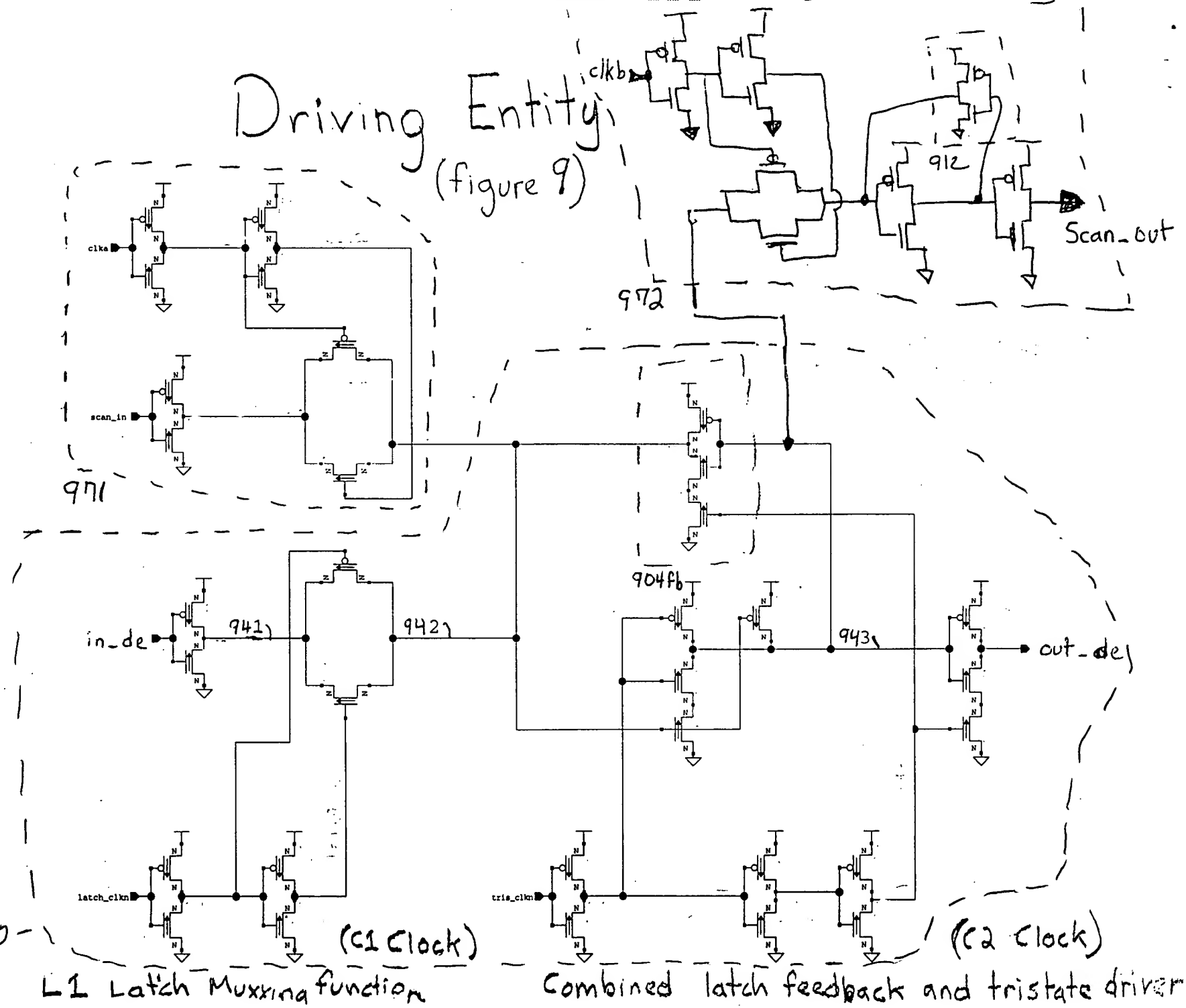


Half Swapper (figure 8)

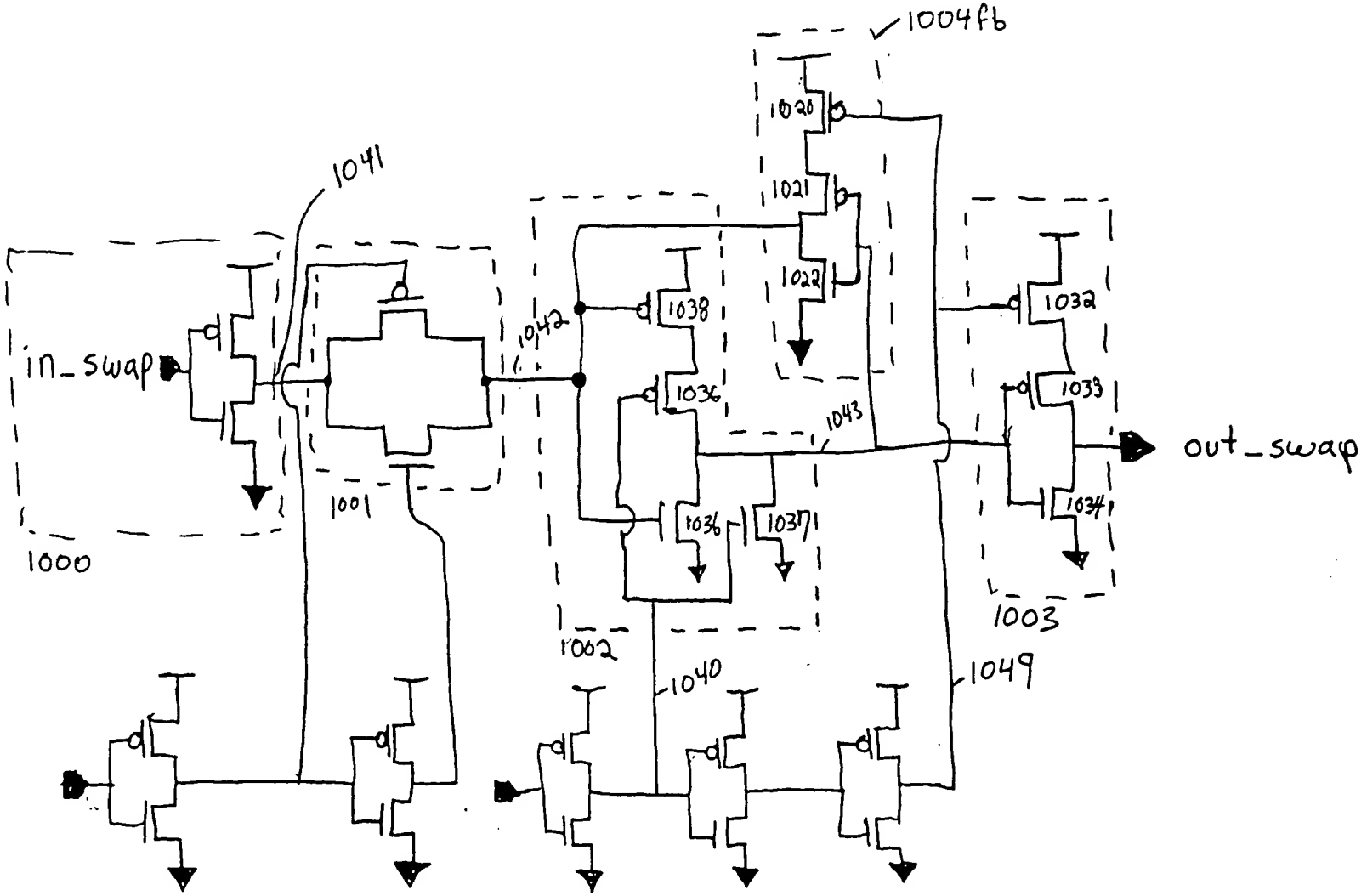


L2 Latch muxxing Function

Combined latch feedback and tristate driver



Half Swapper (figure 10)



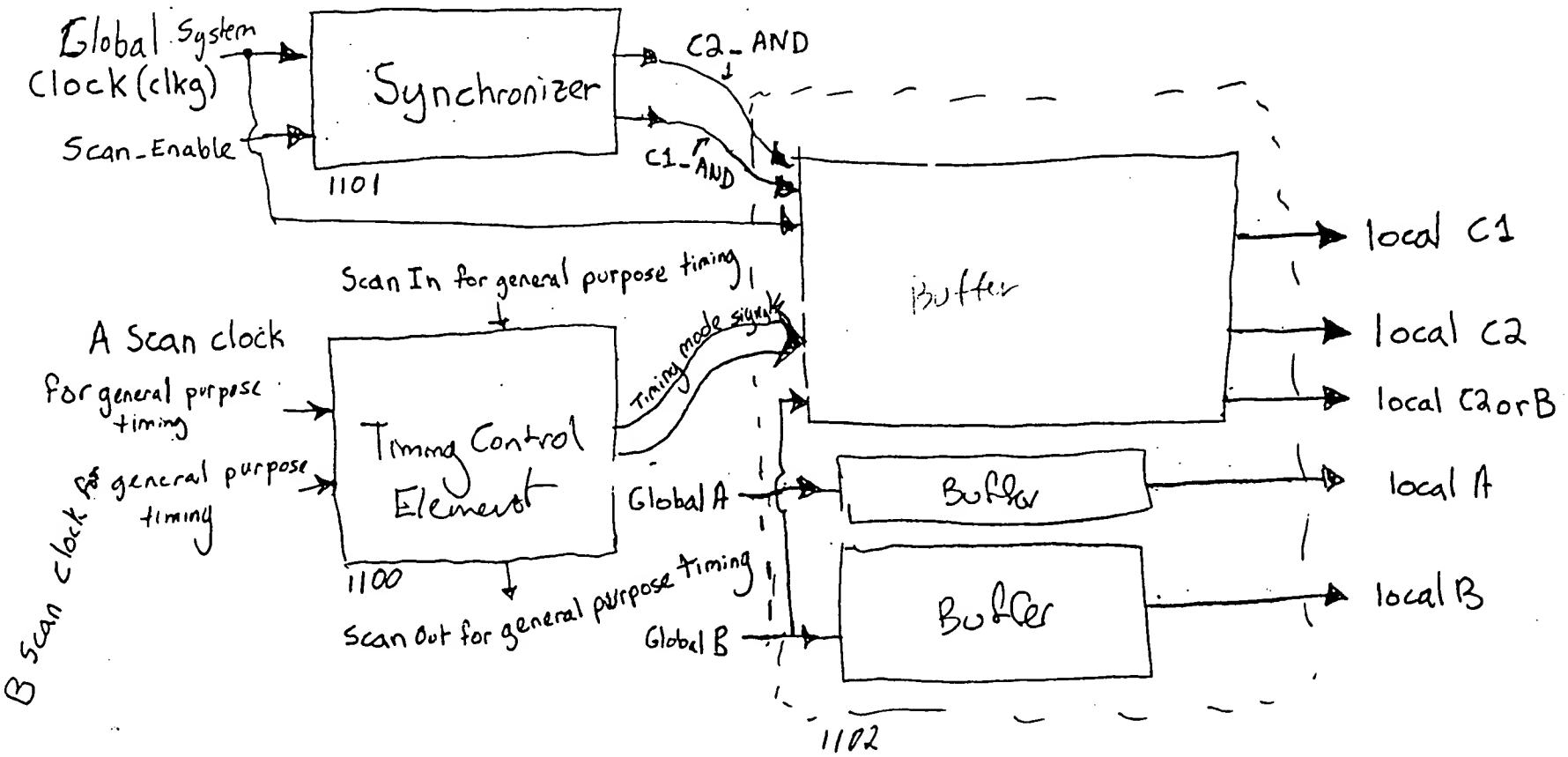

Global System Clock (clkg)
Scan_Enable
Synchronizer
1101
C2_AND
C1_AND
Scan In for general purpose timing
A Scan clock for general purpose timing
B scan clock for general purpose timing
Timing Control Element
1100
Timing mode signal
Scan Out for general purpose timing
Buffer
Global A
Global B
Buffer
Buffer
local C1
local C2
local C2orB
local A
local B
1102

Figure 11

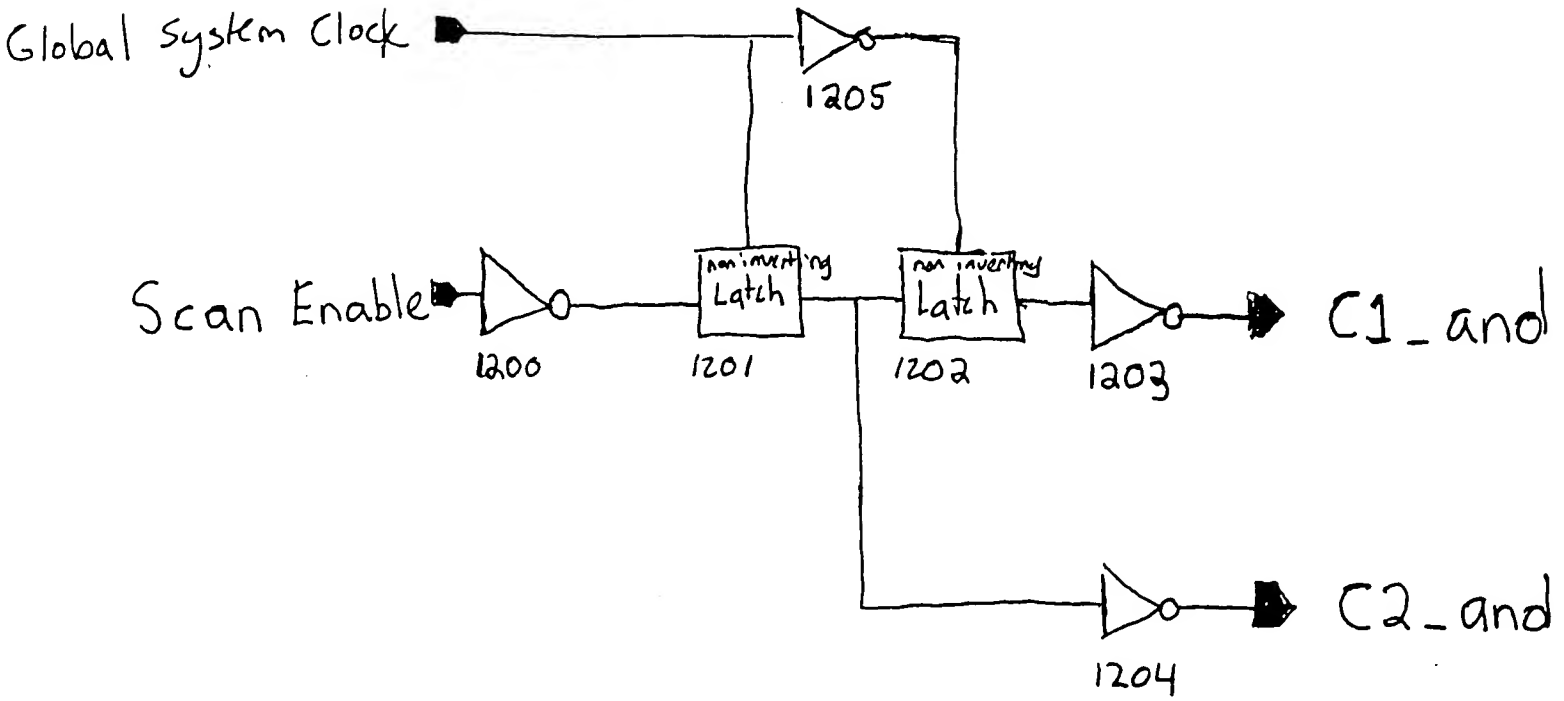


Figure 12

Figure 13

System Clocks for the Driving Entities

(normal operation, = 0)

(approx. power level = 32 driving entities)

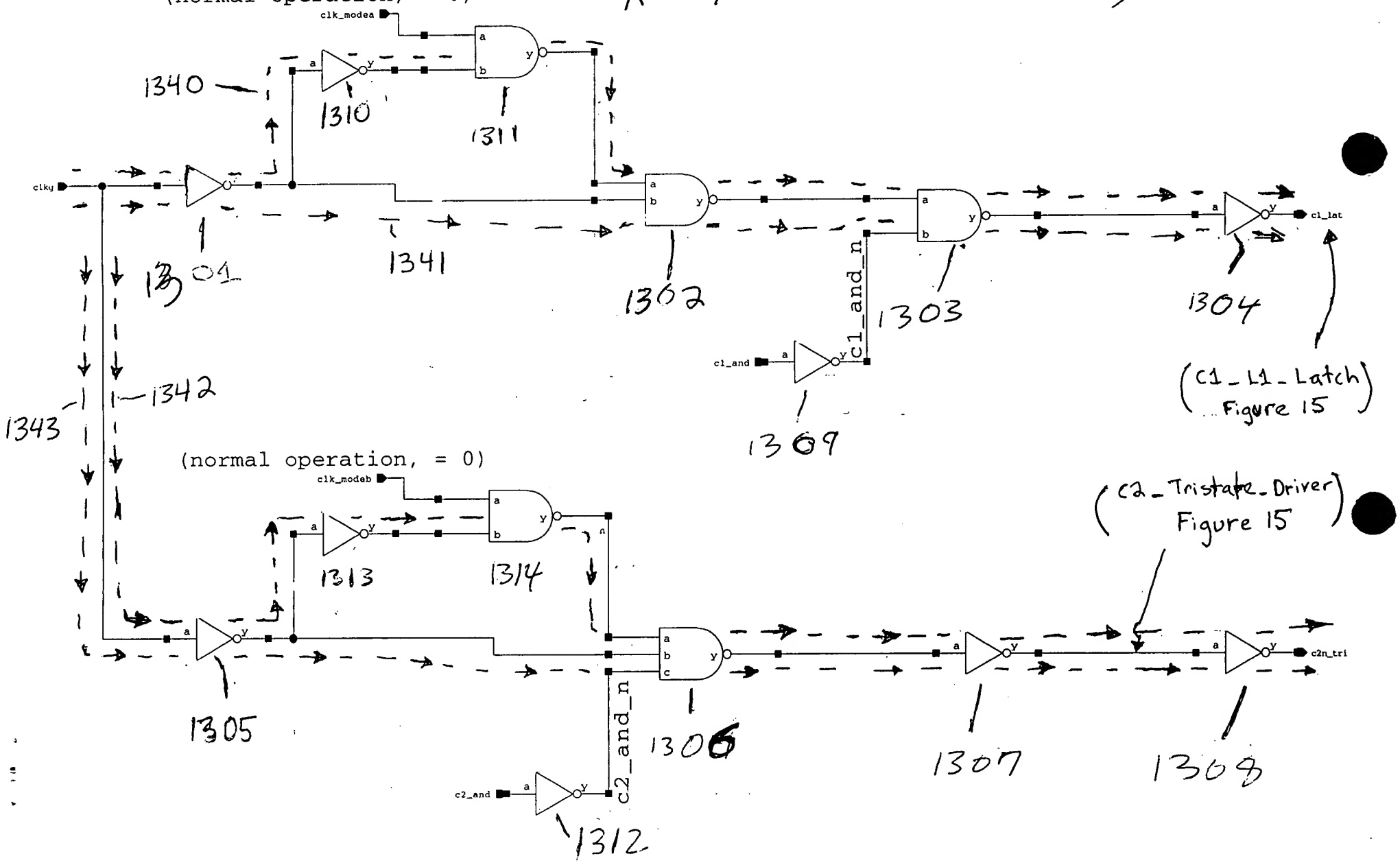
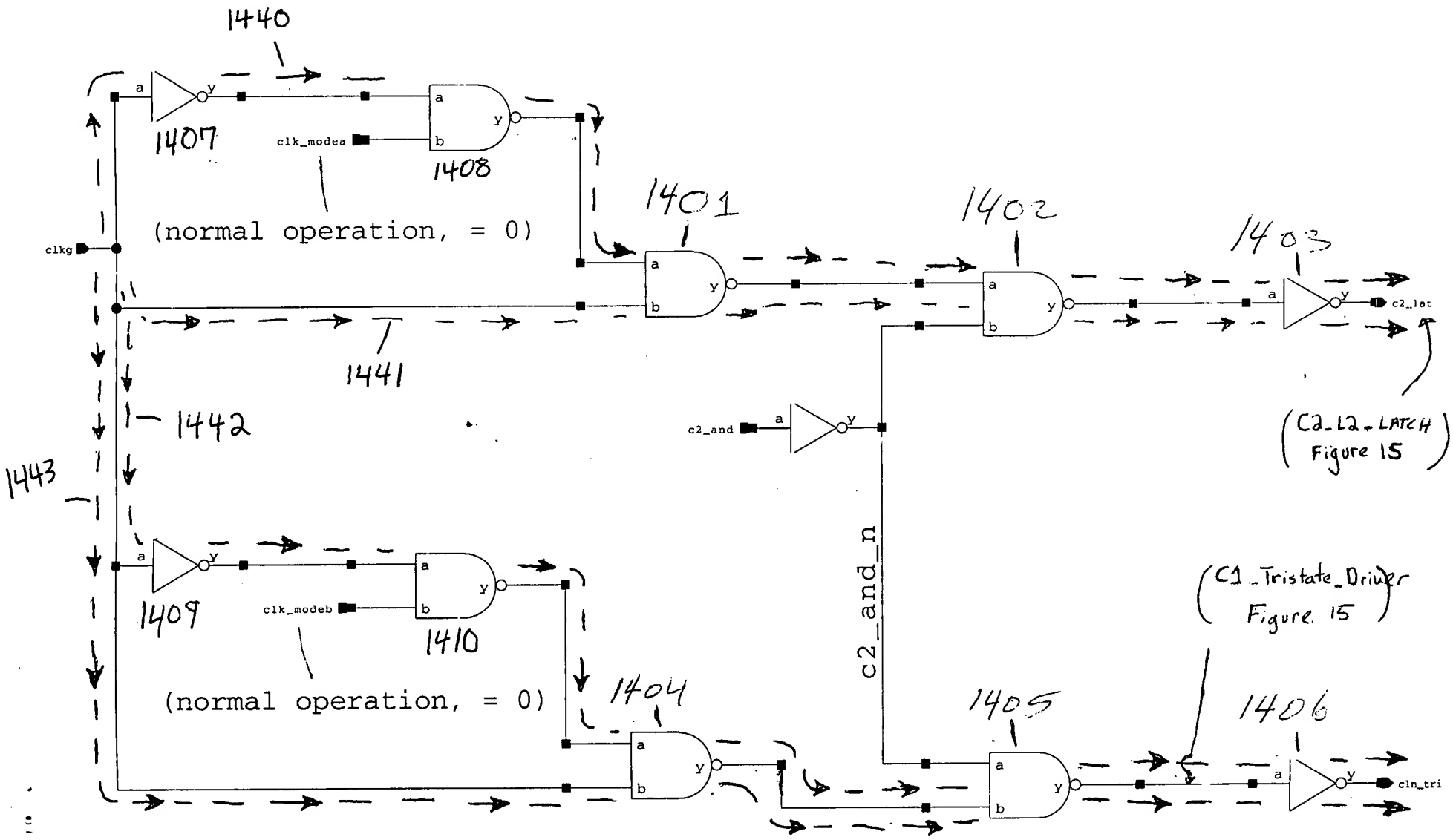


Figure 14

Clocks for the full Swappers

(approx. power level = 32 full swappers)



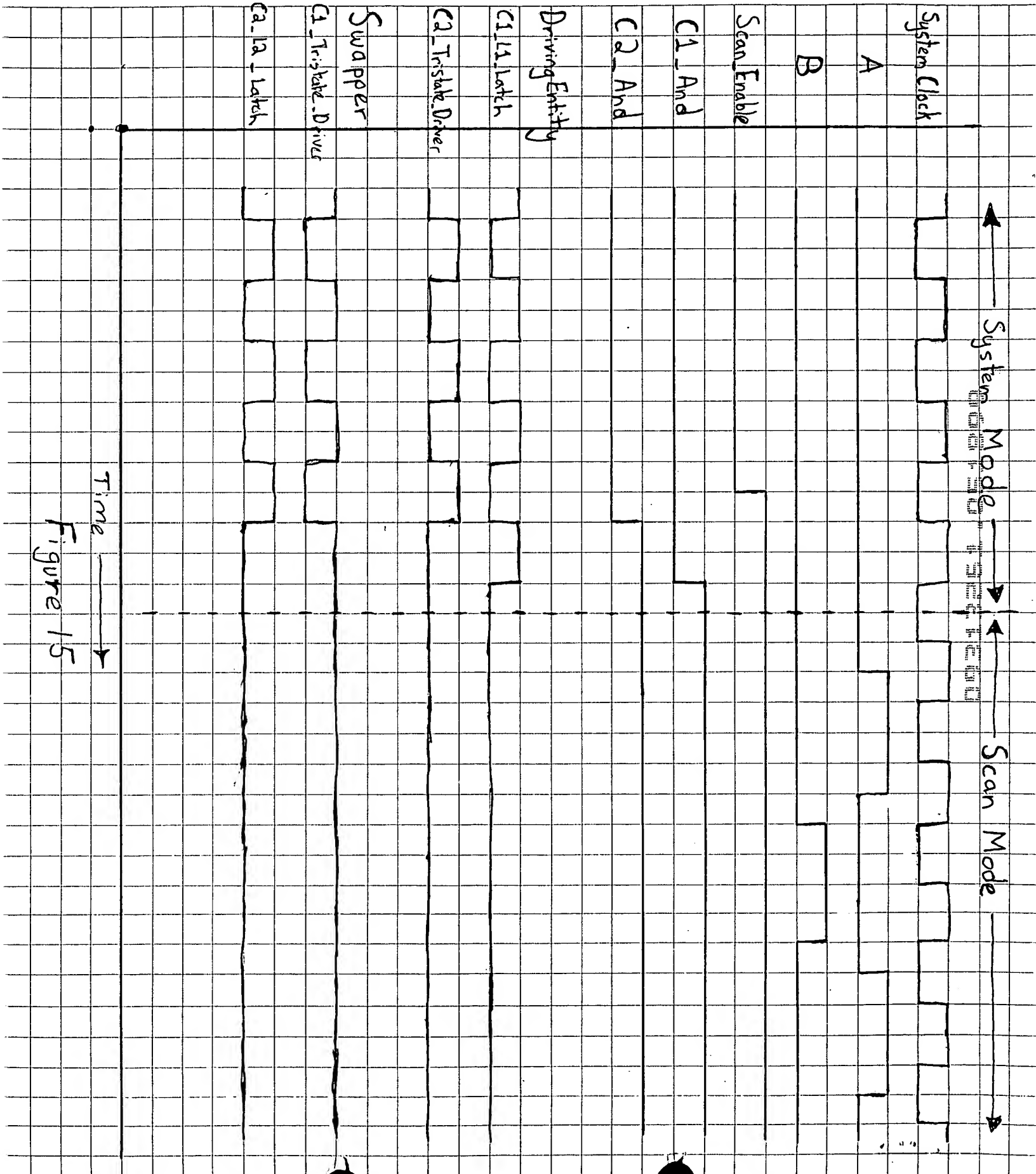


Figure 15

The above understood and witnessed by Date and by Date